

General description

The CD4093 is a 2-input NAND gate with Schmitt-trigger inputs, using advanced CMOS technology. It has good anti-interference ability and strong driving ability.

Features

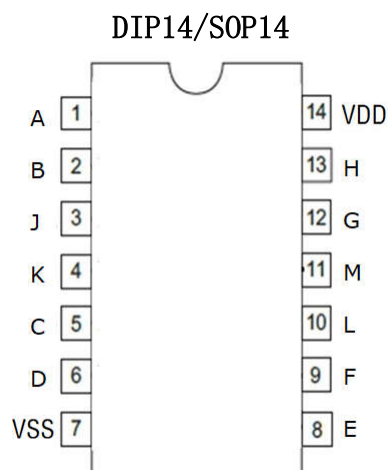
- Low input current: $I_{IN} \leq 1.2\mu A$, @ $V_{IN} = V_{DD} = 18V$, $T_a = 25^\circ C$
- Low static power dissipation: $I_{DD} \leq 1.2\mu A$, @ $V_{DD} = 18V$, $T_a = 25^\circ C$
- wide supply voltage range from 3.0V to 18.0V
- Package: DIP14、SOP14

Applications

- electronic switch
- Signal Oscillator Generator
- Industrial Control Applications
- Other application areas

Pin description

Serial number	Sym	Serial number	Sym
DIP14/SOP14	-bol	DIP14/SOP14	-bol
1	A	14	VDD
2	B	13	H
3	J	12	G
4	K	11	M
5	C	10	L
6	D	9	F
7	VSS	8	E



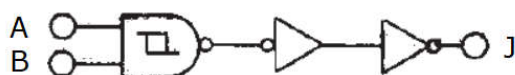
Absolute Maximum Ratings

Parameter	Symbol	Limit value	Unit
Supply voltage	V_{DD}	-0.5-20	V
Input voltage	V_{IN}	-0.5+ $V_{SS} - V_{DD} + 0.5V$	V
Power dissipation	P_D	500	mW
Ambient temperature	T_A	-40-85	$^\circ C$
Storage temperature	T_S	-65-150	$^\circ C$
Welding temperature	T_w	260, 10s	$^\circ C$

Note: Absolute Maximum Ratings refer to the maximum values that must not be exceeded under any conditions. Exceeding these limits may result in physical damage such as product degradation.

Additionally, operation close to these limits does not guarantee proper chip functionality..5

■ Schematic diagram



$$\overline{A} \overline{B} = J$$

Note: 1/4 group

■ Function table

INPUTS		OUTPUTS
B/D/F/H	A/C/E/G	J/K/L/M
L	L	H
L	H	H
H	L	H
H	H	L

Note: 1、H = HIGH voltage level; L = LOW voltage level

2、 $\overline{A}\overline{B}=J$; $\overline{C}\overline{D}=K$; $\overline{E}\overline{F}=L$; $\overline{H}\overline{G}=M$

■ Recommended operating conditions

Parameter	Symbol	Min.	Type	Max.	Unit
Supply voltage	V_{DD}	3		15	V
Input/Output voltage	V_{IN} 、 V_{out}	0		V_{DD}	V
Ambient temperature	T_A	0		60	°C

■ Electrical characteristics

DC Electrical Characteristics: Unless otherwise specified, $T_A=25^{\circ}\text{C}$.

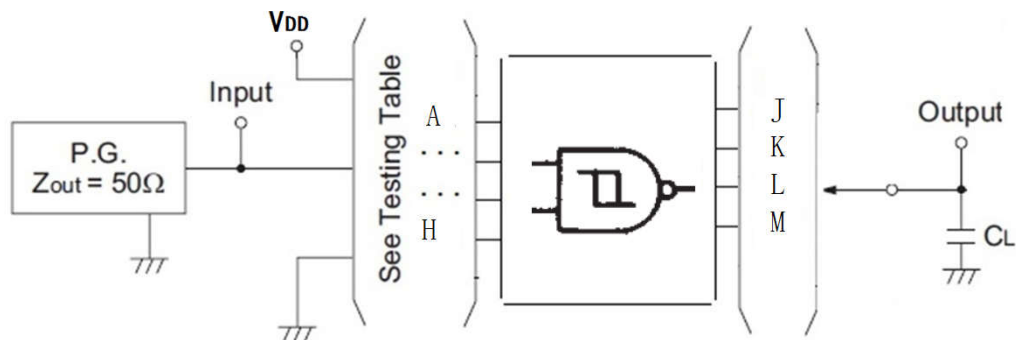
Sym.	Parameter	Conditions	V_{DD} (V)	Min.	Type	Max.	Unit
V_P	Positive trigger threshold voltage		5	—	3.2	4	V
			15	—	8.8	9.5	V
V_N	Negative trigger threshold voltage		5	1.0	1.8	—	V
			15	4.0	5.4	—	V
V_H	Hysteresis voltage Width V_P-V_N		5	—	1.4	—	V
			15	—	3.4	—	V
V_{OH}	HIGH-level output voltage	$ I_{OUT} < 1\mu\text{A}$	5	4.95	—	—	V
			10	9.95	—	—	V
			15	14.95	—	—	V
V_{OL}	LOW-level output voltage	$ I_{OUT} < 1\mu\text{A}$	5	—	0	0.05	V
			10	—	0	0.05	V
			15	—	0	0.05	V
I_{IN}	Input current	$V_{IN}=V_{DD}$ or V_{SS}	18	—	0.01	1.2	μA
I_{OH}	HIGH-level output current	$V_O = 4.6\text{V}$	5	—	-1.8	—	mA
		$V_O = 9.5\text{V}$	10	—	-3.7	—	mA
		$V_O = 13.5\text{V}$	15	—	-13.7	—	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{V}$	5	—	3.6	—	mA
		$V_O = 0.5\text{V}$	10	—	8.6	—	mA
		$V_O = 1.5\text{V}$	15	—	32.5	—	mA
I_{DD}	Static Current	$V_{IN}=V_{DD}$ or V_{SS}	18	—	0.01	1.2	μA

AC Electrical Characteristics: Unless otherwise specified, $T_A=25^{\circ}\text{C}$. For test circuit see next section.

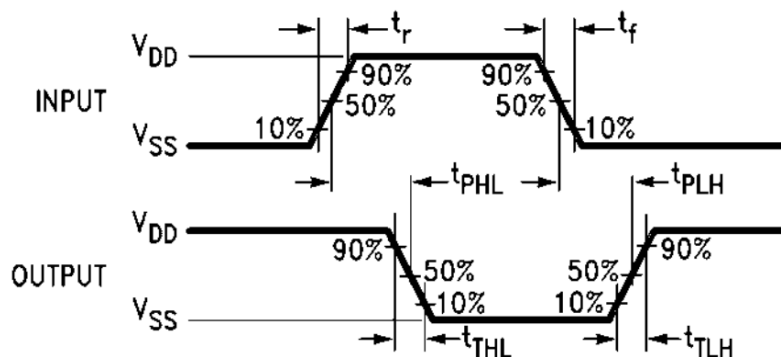
Parameter	Symbol	Conditions	Min.	Type	Max.	Unit
Maximum propagation delay time A or B to J C or D to K E or F to L G or H to M	t_{PHL}	$V_{DD}=5\text{V } C_L=51\text{pF}$	—	130	—	ns
	t_{PLH}		—	85	—	ns
	t_{PHL}	$V_{DD}=10\text{V } C_L=51\text{pF}$	—	70	—	ns
	t_{PLH}		—	50	—	ns
	t_{PHL}	$V_{DD}=15\text{V } C_L=51\text{pF}$	—	60	—	ns
	t_{PLH}		—	35	—	ns
Output Rise Time , Output Fall Time	t_{THL}	$V_{DD}=5\text{V } C_L=51\text{pF}$	—	90	—	ns
	t_{TLH}		—	70	—	ns
	t_{THL}	$V_{DD}=10\text{V } C_L=51\text{pF}$	—	50	—	ns
	t_{TLH}		—	35	—	ns
	t_{THL}	$V_{DD}=15\text{V } C_L=51\text{pF}$	—	40	—	ns
	t_{TLH}		—	25	—	ns

■ Test data

1、Test circuit



2、Waveforms

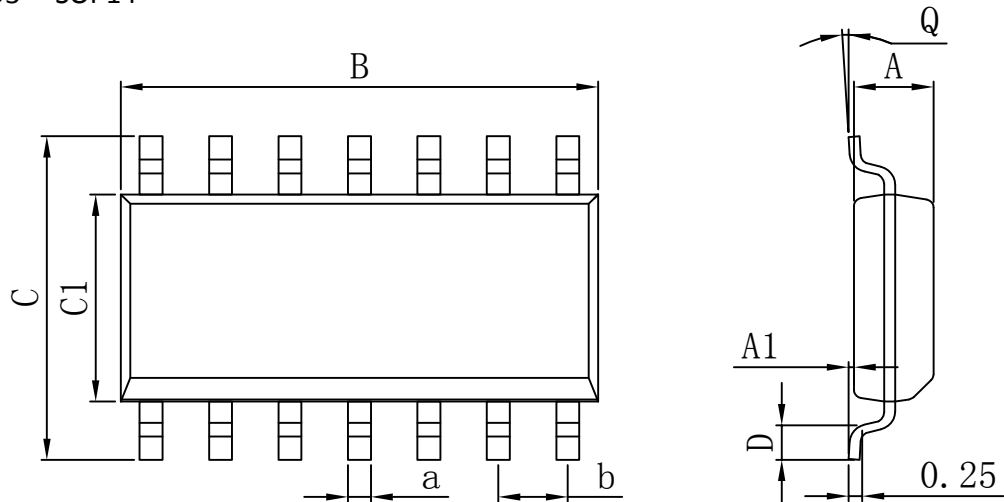


Note:

1. See Testing Table refers to the corresponding test items in the AC electrical characteristics table;
2. C_L capacitor is an external chip capacitor (0603), connected close to the output pin, and the capacitor ground is close to the chip VSS;
3. Input: port input level, $f=1\text{MHz}$, $D=50\%$ square wave, $t_r=t_f \leq 20\text{ns}$;
4. Output: Y-terminal output test.

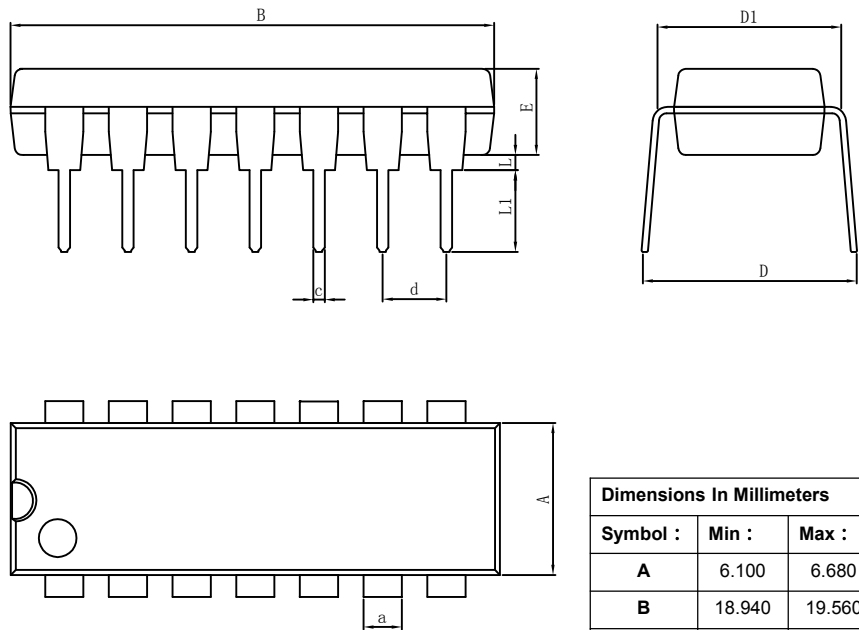
■ Package outline

CD4093 SOP14



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	8.500	9.000	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			

CD4093D DIP14



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	L1	3.000	3.600
D	8.200	9.200	a	1.524 TYP	
D1	7.42	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	